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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,961	04/02/2004	Tan Ba Tran	550-545	7733
23117	7590	10/05/2006	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203				BATAILLE, PIERRE MICHE
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,961	TRAN ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 August 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-6 and 8-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3,5,6,9-12,14,15,17 and 18 is/are rejected.
- 7) Claim(s) 4 8 13 16 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

1. This Office Action is responsive to Applicant's communication filed August 14, 2006 responding to Non-Final rejection mailed April 18, 2006. Applicant's amendment and/or arguments have been considered with the results that follow.
2. Claims 1-6 and 8-18 are now pending in the application under prosecution as claims 7 has been canceled by applicant's amendment.
3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The following is noted:

Claim 9 should be amended because the claim depends upon canceled claim 7. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Response to Arguments

4. Applicant's arguments with respect to claims 1-6 and 8-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-3, 5-6, 9-12, 14-15, and 17-18 are rejected under 35 U.S.C. 103(a) as

being unpatentable over US 4,979,100 (Makris et al) in view of US 6,138,219 (Soman).

With respect to claims 1, 9, 10, 17, and 18, Makris discloses data processing apparatus and method comprising: arbitration logic (Column 18, lines 25-26 - Mention Arbitration Logic); a data processor core, said data processor core comprising: a memory access interface portion for performing data transfer operations between an external data source and at least one memory associated with said data processor core; a data processing portion for performing data processing operations (Column 4, lines 3-66); a read/write port for transferring data from said processor core to at least two buses, said at least two buses providing data communication between said processor core and said at least one memory, said at least one memory comprising at least two portions, each of said at least two buses providing data access to respective ones of said at least two portions, (Column 19, lines 52-58 and Column 20, lines 1-43); wherein said arbitration logic is associated with said read/write port and said arbitration logic routes a data access request requesting access of data in one portion of said at least

one memory received (Column 6, lines 22-37; Column 24, lines 19-36). Makris fails to specifically teach first memory bus and second memory bus providing exclusive access to respective first memory portion and second memory portion such that arbitration logic routes data access request in first memory portion to first data portion and routes data access request in second memory portion to second data portion. However, Soman teaches method of and operating architectural enhancement for multi-port internally cached dynamic random access memory (AMPIC DRAM) systems, eliminating external control paths and random memory addressing, while providing zero bus contention for DRAM access (title abstract), comprising a random access memory (DRAM) architecture connected to a common systems bus interface, the improved DRAM architecture comprising an array of multi-port internally cached DRAM banks (AMPIC DRAM) wherein each DRAM bank being connected to a single destination I/O data read resource port each dedicated to that DRAM bank for respectively storing buffered data destined for that bank and for reading out the stored data solely to the dedicated I/O data read resource port (Column 3, lines 2-14). Therefore it would have been obvious to one of ordinary skill in the art to have combined Makris's and Somans disclosures because the result would have provided multi-port internally cached dynamic random access memory (AMPIC DRAM) systems while eliminating external control paths and providing random memory addressing with providing zero bus contention for DRAM access (title, abstract).

With respect to claims 3, 5-6, 11-12, and 14-15, the combination of Makris and Soman teaches The DRAM bank arbiter, FIG. 2, grants the different serial data interfaces access to the DRAM banks of the AMPIC device, allowing the serial data interfaces to be switched to move the data from the write cache into the proper memory location in the internal DRAM banks (Soman, Col. 4, Lines 36-61); at least two portions of said memory comprise an instruction portion storing instructions and at least one data portion storing data items, said arbitration logic routing said data access request to a first one of said at least two buses providing access to said instruction portion when data to be transferred is an instruction and routing said data access request to a second of said at least two buses providing access to said at least one data portion when data to be transferred is a data item (Makris, Column 29, lines 43-44 and Column 30, lines 1-27); said arbitration logic, in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in one portion of said at least one memory routing said data access request from said memory access interface portion to one of said at least two buses providing data access to said one portion of said at least one memory before routing said request from said processing portion to said one of said at least two buses (Makris, Column 20, lines 44-67); said arbitration logic detecting a wait request from at least one busy portion of said at least one memory, said arbitration logic not routing any data access requests to said busy portion until said wait request is no longer detected (Makris, Column 11, lines 55-68 and Column 12, lines 1-2).

Allowable Subject Matter

8. Claims 4, 8, 13, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,931,479 (Choi) teaching method and apparatus for multi-functional inputs of a memory device.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

September 30, 2006

**PIERRE BATAILLE
PRIMARY EXAMINER**